## AMENDMENTS TO THE SPECIFICATION

Please amend the Specification as follows:

**[0036]** In the embodiment of FIG. 7, a digital input signal x(t), which may be in the form of a serial bit stream, is supplied to a digital filter 46, which implements a mapping function to generate corresponding In-phase and quadrature values I(n) and Q(n) of the complex input signal 34. If desired, the digital filter 46 may also implement a compensation function to electrically pre-compensate impairments of the optical communications system. This functionality is described in detail in application's co-pending United States Patent Applications Nos. 10/262,944 filed October 3, 2002; 10/307,466 filed December 2, 2002; 10/405,236 filed April 3, 2003, and International Patent Application No. PCT/CA03/~~xxxxx~~01044 filed July 11, 2003. Various known digital filter types may be used to implement the digital filter 46, such as, for example, a Random Access Memory Look-up Table (RAM LUT). Alternatively, the digital filter 46 may be implemented using Finite Impulse Response (FIR) filters, Infinite Impulse Response (IIR) filters, and Fast Fourier Transform (FFT filters). In either case, the digital filter 46 generates the In-phase and quadrature signal component values I(n) and Q(n) 35at a sample rate which is about double the bit-rate of the input signal x(t). A non-linear compensator 48 (which may also be implemented as a RAM LUT) is used to adjust the value of each successive sample I(n) and Q(n), by digitally adding successive dither values d1(n) of dither signal d1, and dither values d2(n) of dither signal d2, respectively. The non-linear compensator 48 may also be used to compensate non-linear performance of the complex modulator 30, as described in applicant's co-pending United States Patent Applications No. 10/262,944, filed October 3, 2002; and 10/~~xxx,xxx~~457,528 filed June 10, 2003 entitled "High Speed Digital-to Analog Converter"; and International Patent Application No. PCT/CA03/~~xxxxx~~01044 filed July 11, 2003. The non-linear compensator 48 may be implemented as a separate device cascaded with the digital filter 46, as shown in FIG. 7, or may be "embedded" within the digital filter 46 by applying the dither signals d1 and d2 (and any other mapping function implemented by the non-linear compensator 48) to the digital filter 46.

**[0037]** Respective high-speed Digital-to-Analog Converters (DACs) 50a,50b can then be used to convert the sample values into corresponding analog signals. A high-speed DAC suitable for this purpose is known from applicant's co-pending United States Patent Application No. 10/~~xxx,xxx~~457,528 filed June 10, 2003. If desired, the analog signals can be conditioned, for example by means of respective filters 52a,52b and low noise amplifiers (LNA) 54a,54b, in a conventional manner, to remove out-of-band noise and to scale the signal amplitude to the dynamic range of the complex modulator 30.

## AMENDMENTS TO THE DRAWINGS

Replacement formal drawing pages covering Figures 4a, 4b, 7 and 8 are enclosed, along with a marked-up copy of the replacement drawing pages in which the revisions made have been highlighted.

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|---|---|
| Attachment: | Replacement Sheet(s)<br>Annotated Sheet(s) Showing Changes. |